**Chapter 3**

**Challenges and Solutions in Analog Layout Design**

Analog layout design is a critical step in the development of analog circuits, as it involves creating a physical representation of the circuit that can be fabricated and tested. However, this process can be complex and challenging, as a range of factors can impact the performance of the circuit. In this chapter, we will explore some of the common challenges that can arise in analog layout design, including matching and symmetry, parasitics , crosstalk and electromigration. We will also discuss strategies and techniques for addressing these challenges, including layout by understanding these challenges and approaches to addressing them, designers can create analog layouts that meet the required performance specifications and are manufacturable.

***One of the most prominent challenges in analog layout Mismatch problem***

**Mismatching in (IC) integrated circuits is generally of two types:**

* **Random mismatches:** the error resulting from that one can’t be identified or controlled while implementing the layout, it will happen during the fabrication and the reasons behind that are the non-uniform etch rate, the doping and finally the wafer itself. errors by variations in the thickness of oxide layers, variations in the doping level of transistors, and variations in the width and length of metal interconnects. These variations can lead to differences in the performance of individual components, even when the components are designed to be identical
* .**Systematic mismatches :** which is due to non-uniform thermal distribution during fabrication process, it can be solved by proper layout techniques, best device matching so as to be as close as possible to the needed performance. Systematic mismatches are caused by: Process biases, Mechanical stress, Temperature gradients, and Polysilicon etch rates, etc.

**What is matching?**

Two integrated device or more have same desired value are exposed to the same conditions whether pressure, temperature, current etc.

**Why needs matching?**

What if your headphones started playing songs with more volume in left than the right? Sounds bad right. So, the voice sensitivity needs to be matched for both left & right side by same.

Actually, due to process variation in fabricating the transistors (like non uniform doping, oxide thickness, etching etc.), no 2 transistors have exactly the same electrical properties. By applying techniques such as Interdigitzer & Common centroid, it is possible to match transistors reasonably

In a sensitive amplifier (differential pair), matching would greatly enhance the performance by improving the ability to reject noise in its differential input.

**How to do matching?**

We can achieve matching when avoid mismatch sources and use relative accuracy Mismatch is a deviation of values of integrated component after fabrication desired value used for simulation Let’s assume we want design low pass filter in 1MHZ

in simulation design ,

after fabrication process , ,

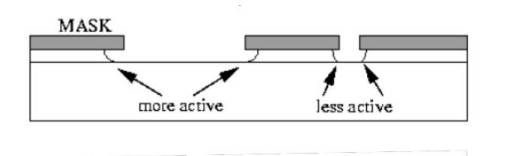
**We will identify the most prominent sources of mismatch**

* Process Variations
* Placement and Gradient

**Mismatch (Process variations)**

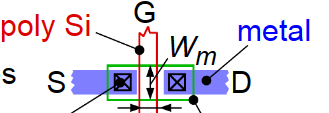
Process variation during fabrication process limits accuracy and desired performance of analog circuit:

* + **mask production and alignment**
  + **latera diffusion**: Diffusion widens implanted region can affect doping of neighboring devices. Solution: Increase distance and use dummy structures that affect all transistors the same.
  + **over etching**: Poly silicon does not always etch uniformly.

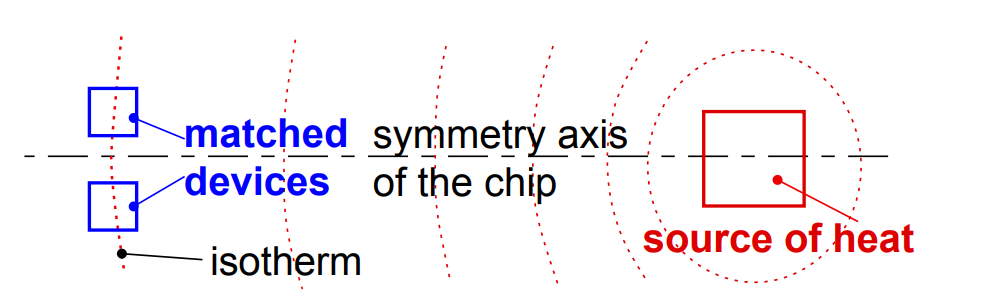


* + Large openings etch faster than small openings in mask. Solution: is to use dummy structures.

And all of this effects on Dimensions of device Ratio and consequently the threshold voltage value will change with it.



* Mismatch (Placement and Gradient)
* Orientation
* Stress gradient: occurs mainly from wafer dicing where stress is highest at edge of the chip, Packaging can cause stress in chip. **Solution:** Keep critical matched devices in center of chip, avoid using corners for matched devices
* Temperature gradient We use matching so that the devices are exposed to the same thermal effect



The devices have the same orientation, are close to each other, and are interleaved as neighbors to each other. We have satisfied the three main rules, When these components are etched, the ones in the middle of the block see very different conditions during processing than the ones on the ends. The resistors on the ends might etch more, making them slightly narrower than the ones in the middle



Figure 4 1Edges of blocks etch differently than middles of blocks.

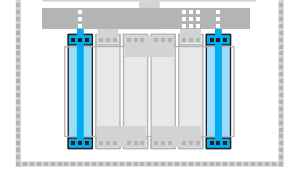
To reduce the impact of process variations and parasitics (will be illustrated) and improve performance we use dummy components.

Figure 4 2 Two dummies to help the four circuit resistors etch

**Dummy components**, also known as "fillers," are non-functional components that are added to the layout of an integrated circuit to improve performance and reduce the impact of process variations and parasitics. They are typically made of the same materials as the functional components and are designed to match the physical characteristics of the functional components. There are several types of dummy components that can be used in layout design, including dummy resistors, dummy capacitors, dummy transistors, These components are strategically placed in the layout to achieve specific goals, such as matching the resistance . Dummy resistors are often used in analog layout design to match the resistance of functional resistors and reduce the impact of process variations. They are typically placed in parallel with the functional resistors and have the same dimensions and materials as the functional resistors. Dummy transistors are non-functional transistor structures that are added to the layout to match the parasitic capacitance and resistance of functional transistors and reduce the impact of process variations. They are typically placed in parallel with the functional transistors and have the same dimensions and materials as the functional transistors. designers can identify the optimal placement and number of dummy components to achieve optimal performance. Notice we shorted the dummy resistors together and tied them to ground or (VDD). They are not part of the circuit. They are only there to give the outer two circuit resistors similar conditions for etching as the inner two circuit resistors.

dummies are used to balance the effects on the lateral transistors, they may be used as well to shield all around the devices in smaller and more sensitive technologies.

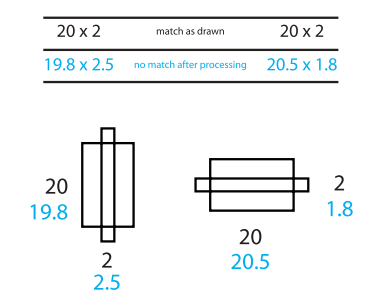
Before talking about matching techniques let’s see the Rules for MOS transistor matching:

**Rules for optimum matching:**

1. **Minimum distance**
2. **Same surroundings (same neighborhood)**

When we see in this figure of two transistor, we see that the transistors have been placed directly next to each other. Good in terms of distance however, if you continue thinking about these two transistors, you notice another problem.

For a CMOS transistor, the parameters that most affect the characteristics of the transistor are the gate length (L)and the gate width(W). Some etches used in processing etch preferentially in one direction. That is the problem. One device is placed sideways. What etching errors occur in one transistor’s width, will occur in the other transistor’s length.

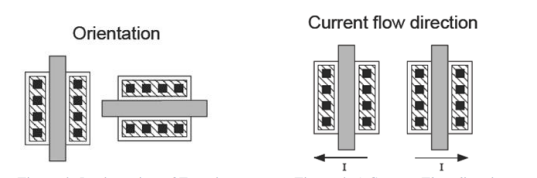


After etching process, we found one device width equal 20.5 and other 19.8

1. **Same orientation on the chip**

If we follow these three basic rules, throughout all of our layout, we are guaranteed a certain amount of good matching, plus the advantage of better device performance. There will be times when trying to keep all our transistors, resistors, and capacitors in the same orientation makes your layout very difficult in this case can split up and reshape our devices, there will be times when we cannot split our devices sensibly, or we are not allowed to. In these cases, how much we know about what the circuit is doing can help our layout. Find out what components are the least important in the circuit and maybe, just maybe they can be rotated to make your layout smaller.

For example, you might have a problem device that just will not fit well in our layout. If you think the device is non-critical, it may be a good to rotate. Go to our circuit designer and ask, “Is it ok to rotate this transistor?” communicate with our circuit designer help us to find suitable solutions.

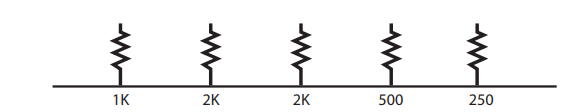


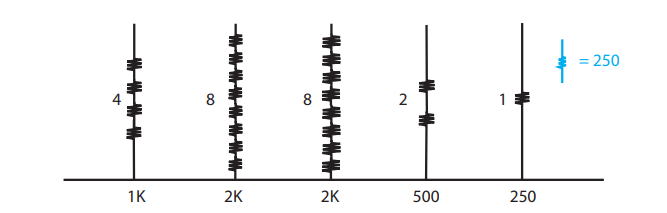
1. **choose appropriate unit to be used in matching**

Sometimes we have more than two devices that must match each other. There might be five or six devices, all needing to match.

First step we can use is placing the resistors as close together as we can, second step is to keep them in the same orientation, third step is called a root component I mean one resistor from which you will make all the others. Using a root component, if the resistors are all the same size, all the same shape, and all the same orientation, and they are all close to each other, you get very good matching. If the resistors over-etch, they all over-etch the same way and still match each other.

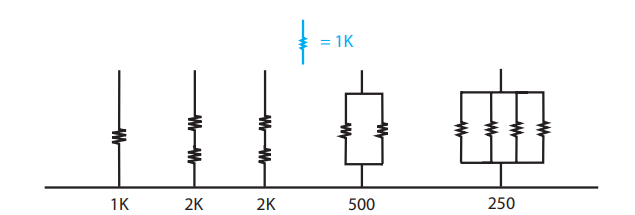
For example





if use It is good but in this example we have some large resistors, like the resistor, for instance. Consider this, contacts on a resistor are typically quite variable and using a resistor as the root component could have a significant portion of its resistance made up from contact resistance. The contact resistance could then create a significant amount of the total resistance on your larger resistors, which have eight times the number of contacts.

So, we Choose a middle value for our root component:



If use 1k better way to use the root component strategy is to pick a medium value. Let’s pick one from our previous example. Let’s choose 1K as our root resistor. The 2K’s would each be two resistors in series. The 500-ohm is two resistors in parallel, and the 250 would be four resistors in parallel. We have made all our required values based on a 1K resistor. We used both series and parallel arrangements.

The root device method can be used with any type of device, not only resistors. The same issues.

**Summery Rules for optimum matching:**

Devices to be matched should have:

1. Same structure
2. Same temperature
3. Same shape and same size
4. Minimum distance,
5. use relative accuracy not absolute(true) accuracy.
6. choose appropriate unit size.

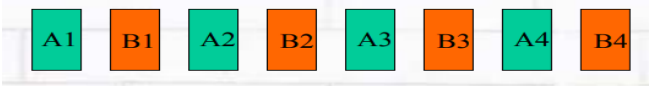
**How the matching method is actually applied?**

There are two common way :

1. **inter-digitiation**
2. **common centroid**

Let's say we have two devices A,B )A and B can be anything likes transistor, resistor, and capacitor) and split A and B into 4 small multiplier A1-A4 and B1-B4.

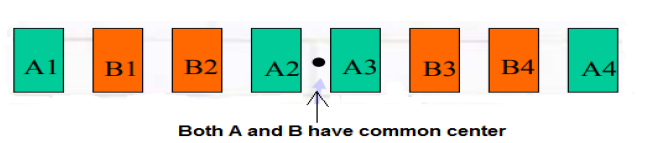
Center of **A2B2** and **A3B3**



Center of **A1B1** and **A2B2**

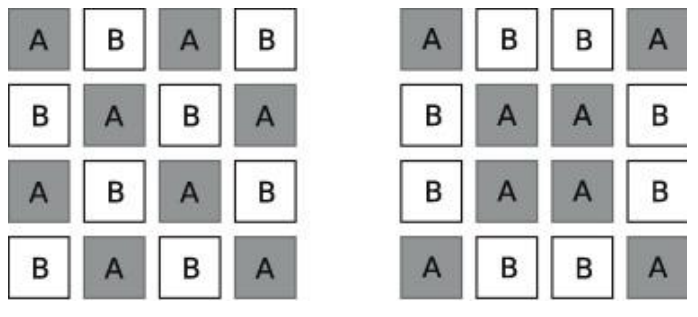
Center of **A3B3** and **A3B4**

**Inter-digitization technique**: Placing alternate components.



**Common centroid technique**: all components have same centroid.

Example of the two way



Inter-digitation common centroid